IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a semiconductor substrate having a cell array region and a peripheral circuit region;

a plurality of word line patterns placed on the cell array region, the word line patterns including a word line and a word line capping layer;

at least one gate pattern placed on the peripheral circuit region;

an interlayer insulating layer covering an upper surface of the semiconductor substrate having the word line patterns and the at least one gate pattern;

a self-aligned contact hole formed in the interlayer insulating layer between the word line patterns;

a self-aligned contact spacer covering a side wall of the self-aligned contact hole; and

gate spacers interposed between side walls of the at least one gate pattern and the interlayer insulating layer, a width of the gate spacers being substantially different from a width of the self-aligned contact spacer.

2. (Currently amended) The semiconductor device according to claim 1, further comprising:

word line spacers interposed between side walls of the word line patterns placed opposite to the self-aligned contact hole and the interlayer insulating layer, the word line spacers being formed of the same material layer as the gate spacer, ~~the word line spacers having the same width as that of the gate spacers~~ a maximum width of the word line spacers substantially the same as a maximum width of the gate spacers.

3. (Currently amended) The semiconductor device according to claim 2, further comprising:

a spacer etch stop layer ~~interposed between~~ disposed in contact with the word line spacers and the word line patterns in the cell array region, ~~between~~ disposed in contact with the gate spacers and the at least one gate pattern in the peripheral circuit region, and ~~between~~ disposed in contact with the self-aligned contact spacer and the word line patterns in the cell array region.

4. (Currently amended) The semiconductor device according to claim 2, further comprising:

a contact etch stop layer ~~interposed between~~ disposed in contact with the word line spacers and the interlayer insulating layer in the cell array region, and ~~between~~ disposed in contact with the gate spacers and the interlayer insulating layer in the peripheral circuit region.

5. (Currently amended) The semiconductor device according to claim 1, wherein the interlayer insulating layer is one selected from the group consisting of an HDP oxide layer, a USG layer, ~~a BPSG layer,~~ and a PSG layer.

6. (Currently amended) The semiconductor device according to claim 1, ~~wherein~~ the self-aligned contact hole ~~includes~~ comprising a lower contact hole and an upper contact hole, the lower contact hole formed at a region between the word line patterns and having a first diameter, ~~and an~~ the upper contact hole placed on the lower contact ~~hole~~ hole, ~~and formed~~ disposed to penetrate the interlayer insulating layer, and having a second diameter that is unequal to the first diameter.

7. (Currently amended) The semiconductor device according to claim 6, ~~wherein the diameter of the lower contact hole is less than that of the upper contact hole~~ the second diameter greater than the first diameter in a direction across the word line patterns.

8. (Original) The semiconductor device according to claim 1, wherein the width of the self-aligned contact spacer is smaller than the width of the gate spacers.

9. (Currently amended) A device comprising:

at least two word line patterns in a cell array region of a semiconductor substrate;

at least one gate pattern in a peripheral circuit region of the semiconductor substrate;

an inter-layer insulating layer covering the semiconductor substrate, the at least two word line patterns, and the at least one gate pattern, the at least one gate pattern including a gate spacer, the gate spacer disposed entirely ~~interposed~~ between a sidewall of the at least one gate pattern and the inter-layer insulating layer;

a self-aligned contact hole penetrating the inter-layer insulating layer between the at least two word line patterns; and

a self-aligned contact spacer on a sidewall of the self-aligned contact hole, a width of the self-aligned contact spacer unequal to a width of the gate spacer.

10. (Original) The device of claim 9, further comprising:

a word line spacer between one of the at least two word line patterns and the interlayer insulating layer, the word line spacer formed of the same material and having the same width as the gate spacer.

11. (Original) The device of claim 10, further comprising:

a spacer etch stop layer between the word line spacer and one of the at least two word line patterns, between the gate spacer and the at least one gate pattern, and between the self-aligned contact spacer and the at least two word line patterns.

12. (Original) The semiconductor device according to claim 10, further comprising:

a contact etch stop layer between the at least two word line spacers and the inter-layer insulating layer, and between the gate spacer and the inter-layer insulating layer.

13. (Original) The semiconductor device according to claim 9, the self-aligned contact hole comprising:

a lower contact hole; and

an upper contact hole, a diameter of the upper contact hole greater than a diameter of the lower contact hole in a direction perpendicular to the at least two word line patterns.

14-20. (Cancelled)